WHAT IS CLAIMED IS:

1. A method of manufacturing a NAND flash memory device, comprising the steps of:

providing a semiconductor substrate in which a plurality of isolation films are formed in parallel to each other, a source select transistor having a cell source region, a plurality of memory cells having a cell impurity region and a drain select transistor having a cell drain region are serially connected and formed in each of a plurality of strings in a cell region, and a peri-transistor having a source/drain junction is formed in a peripheral circuit region;

forming a first interlayer insulating film on the resulting semiconductor substrate;

etching a portion of the first interlayer insulating film to expose the cell source regions and the isolation films between the regions, and then etching the exposed portions of the isolation films to form a common source line contact hole through which the semiconductor substrate is exposed;

performing an ion implantation process to form an ion implantation region on the exposed semiconductor substrate at the bottom of the common source line contact hole; and

burying a conductive material within the common source line contact hole in which the ion implantation region is formed, thus forming a common source line.

2. The method of claim 1, before the step of forming the first interlayer insulating film, further comprising the step of forming an etch-stop film having a higher etch selective ratio than that of the first interlayer insulating film on the resulting semiconductor substrate.

3. The method of claim 2, wherein the step of forming the common source line contact hole comprises the steps of:

etching a portion of the first interlayer insulating film to expose the etch-stop film; and

etching the exposed etch-stop film to expose the cell source regions and the isolation films between the regions and then etching the exposed isolation films to expose the semiconductor substrate.

4. The method of claim 1, wherein the common source line contact hole includes, at its bottom, a continuous conductive line consisting of the cell source regions and the ion implantation regions formed between the cell source regions.

5. The method of claim 1, wherein the impurity ion implantation process is performed at a dose of 1E12 to 1E14 atom/cm^2 with an implantation energy of 15keV to 25KeV, using arsenic or phosphorous as an impurity ion.

6. The method of claim 5, wherein the impurity ion implantation process is performed simultaneously with tilt implantation.

7. The method of claim 6, wherein, at the time of the tilt implantation, a wafer is rotated.

8. The method of claim 1, wherein the step of forming the common source line comprises the steps of:

depositing a doped polysilicon as the conductive material on the first interlayer insulating film so that the common source line contact hole, in which the ion implantation region is formed, is buried; and

etching the deposited doped polysilicon layer until the first interlayer insulating film is removed to a given thickness by means of a blanket etch process.

9. The method of claim 8, wherein the blanket etch process is performed until the top surface of the source select transistor is exposed.

10. The method of claim 1, after the step of forming the common source line, further comprising the steps of;

forming a second interlayer insulating film on the first interlayer insulating film including the common source line;

forming a trench etch-stop film and a trench insulating film on the second interlayer insulating film sequentially;

forming a plurality of damascene patterns simultaneously by means of a damascene process; and

burying a metal within the damascene patterns to form a metal wire connected to the common source line, a bit line connected to the cell drain region, a metal wire connected to a gate of the peri-transistor, and a metal wire connected to the source/drain junction of the peri-transistor, separately.